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In the claims:

The claims are as follows:

1. (original) A memory card, comprising:

a first interface controller operable to be coupled to a first interface, said first interface operating to receive database input signals;

a second interface controller operable to be coupled to a second interface, said second interface operating to couple said memory card to a bus;

a first memory interface disposed between said first interface controller and a memory block;

a second memory interface disposed between said memory block and said second interface controller; and

an arbiter coupled to said first and second memory interfaces for arbitrating data input operations and data output operations with respect to said memory block.

2. (original) The memory card as set forth in claim 1, wherein said first interface comprises a network interface coupled to a switch fabric disposed in a telecommunications node.

3. (original) The memory card as set forth in claim 2, wherein said switch fabric comprises an Ethernet fabric.

4. (original) The memory card as set forth in claim 1, further comprising an error correct module coupled to said memory block.

5. (original) The memory card as set forth in claim 1, further comprising a synchronization logic block, said synchronization logic block operating, responsive to a data synchronization signal, to synchronize said data input operations with respect to said memory block with data input operations associated with another memory card.

6. (original) The memory card as set forth in claim 1, wherein said memory block comprises at least one dynamic random access memory (DRAM) module.

7. (original) The memory card as set forth in claim 1, wherein said memory block comprises at least one static random access memory (SRAM) module.

8. (original) The memory card as set forth in claim 1, wherein said memory block comprises at least one high speed, high density non-volatile memory (NVM) module.

9. (original) The memory card as set forth in claim 1, wherein said bus comprises a system bus operating to interconnect a plurality of processor cards disposed in a system shelf.

10. (original) The memory card as set forth in claim 9, wherein said system bus comprises a Compact Peripheral Component Interconnect (CPCI) bus.

11. (original) The memory card as set forth in claim 9, wherein said system shelf forms at least a portion of a telecommunications node.

12. (original) A system for updating a distributed database associated with a telecommunications node, comprising:

a database update manager for generating database update signals indicative at least of updated data; and

at least one memory card disposed in a system shelf forming a portion of said telecommunications node, said at least one memory card cooperating with a network interface for receiving said database update signals through a switch fabric, wherein said at least one memory card is operable to contain at least a portion of said distributed database in a memory block disposed thereon.

13. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 12, further comprising a synchronization signal generator associated with said database update manager, wherein said synchronization signal generator is operable to provide a data update synchronization signal for synchronizing said database update signals provided to a plurality of said memory cards.

14. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 13, wherein said synchronization signal generator is integrated with said database update manager.

15. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 12, wherein said database update manager is co-located with said telecommunications node.

16. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 12, wherein said switch fabric comprises an Ethernet fabric.

17. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 12, wherein said memory block comprises a dynamic random access memory (DRAM) module.

18. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 12, wherein said memory block comprises a static random access memory (SRAM) module.

19. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 12, wherein said memory block comprises a non-volatile memory (NVM) module.

20. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 12, wherein said at least one memory card comprises:

a network interface controller operable to be coupled to said network interface;

a bus interface controller operable to be coupled to a system bus interface, said system bus interface operating to couple said at least one memory card to a system bus;

first and second memory interfaces associated with said memory block, wherein said first memory interface is disposed between said network interface controller and said

memory block and said second memory interface is disposed between said bus interface controller and said memory block; and

an arbiter coupled to said first and second memory interfaces for arbitrating data update operations and data output operations with respect to said memory block.

21. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 20, wherein said at least one memory card further comprises an error correct module coupled to said memory block.

22. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 20, wherein said system bus is operable to interconnect a plurality of processor cards.

23. (original) The system for updating a distributed database associated with a telecommunications node as set forth in claim 22, wherein said system bus comprises a Compact Peripheral Component Interconnect (CPCI) bus.

24. (original) A telecommunications node having a distributed database, comprising:

a database manager for generating signals indicative at least one of updating and entering data with respect to said distributed database;

a switch fabric interconnecting a plurality of system shelves; and

a memory card disposed in each system shelf, said memory card cooperating with a network interface for receiving said signals through said switch fabric and with a bus interface for outputting data on a system bus, wherein said memory card is operable to contain at least a portion of said distributed database in a memory block disposed thereon.

25. (original) The telecommunications node having a distributed database as set forth in claim 24, wherein said switch fabric comprises an Ethernet fabric.

26. (original) The telecommunications node having a distributed database as set forth in claim 24, further comprising a synchronization signal generator associated with said database manager, wherein said synchronization signal generator is operable to provide a data synchronization signal for synchronizing database input operations with respect to said memory cards.

27. (original) The telecommunications node having a distributed database as set forth in claim 24, wherein said memory block comprises at least one dynamic random access memory (DRAM) module.

28. (original) The telecommunications node having a distributed database as set forth in claim 24, wherein said memory block comprises at least one static random access memory (SRAM) module.

29. (original) The telecommunications node having a distributed database as set forth in claim 24, wherein said memory block comprises at least one non-volatile memory (NVM) module.

30. (original) The telecommunications node having a distributed database as set forth in claim 24, wherein said system bus comprises a bus segment operating to interconnect a plurality of processor cards.

31. (original) The telecommunications node having a distributed database as set forth in claim 30, wherein said bus segment comprises a Compact Peripheral Component Interconnect (CPCI) bus segment.

32. (original) The telecommunications node having a distributed database as set forth in claim 24, wherein said memory card comprises an error correct module coupled to said memory block.

33. (original) The telecommunications node having a distributed database as set forth in claim 24, wherein said memory card comprises:

a network interface controller operable to be coupled to said network interface;

a bus interface controller operable to be coupled to said bus interface;

first and second memory interfaces associated with said memory block, wherein said first memory interface is disposed between said network interface controller and said memory block and said second memory interface is disposed between said bus interface controller and said memory block; and

an arbiter coupled to said first and second memory interfaces for arbitrating data input operations and data output operations with respect to said memory block.